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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,183	08/25/2003	Byung-Seop Hong	51876P352	5151

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EXAMINER


DANG, TRUNG Q

ART UNIT	PAPER NUMBER
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2823

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,183	HONG ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2,8,14 and 15 is/are rejected.
- 7) ☒ Claim(s) 3-7,9-13 and 16-23 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/25/03</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Wu (U.S. Pat. 6,455,383).

Wu teaches a method for fabricating a semiconductor device comprising the steps of: forming a stack layer of a gate oxide layer (301a), a poly-silicon layer (302a), a tungsten layer (306a), and a hard mask (307a) sequentially deposited on a semiconductor substrate (300); selectively oxidizing only the poly-silicon layer

(302a) of the stack layer; depositing a gate sealing nitride layer (312a) on the selectively oxidized stack layer; and performing a rapid thermal annealing (RTA). See Fig. 4D(a) and related text for the materials of layers 301a, 302a, 306a, and 307a. See col. 9, lines 27-29 for the claimed step of selectively oxidizing only the poly-silicon layer (302a) of the stack layer to form oxide layer 309a in Fig. 4E(a). See paragraph bridging column 9 and column 10 for the claimed steps of depositing a gate sealing nitride layer (312a) (Fig. 4F(a)) on the selectively oxidized stack layer and heat treating the stack layer. Note that, the rapid thermal annealing (RTA) (corresponds to the claimed limitation "heat treating") to redistribute implanted doping impurities (col. 10, lines 1-2) would inherently release stress exerted during the selective oxidizing and gate sealing nitride layer depositing, absent evidence to the contrary.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu as above in view of Quek et al. (U.S. Pat. 6,214,680) and RD 290097 A (foreign patent document).

Wu teaches a method for fabricating a semiconductor device as noted above.

Wu differs from the claim in not disclosing that the selective oxidizing and the heat treating (read on by the RTA in Wu) are carried out in two different LPCVD furnaces under an ex-situ method.

Quek et al. teach that a grown oxide (i.e., an oxide formed by thermally grown on a substrate) can be formed by rapid thermal oxidation (RTO), low pressure chemical vapor deposition (LPCVD) or furnace oxidation (col. 3, lines 17-19).

RD 290097A teaches that electrical activation (or redistribution of implanted doping impurities) can be carried out in a LPCVD furnace, an annealing furnace or a rapid thermal annealing apparatus (last paragraph of Abstract).

It would have been obvious to one of ordinary skill in the art to carry out the selective oxidizing and annealing processes of Wu in two different LPCVD furnaces because oxidation and annealing processes are known to be carried out in LPCVD furnaces as suggested by Quek and RD 290097A, and the application of a known process to make the same would have been within the level of one skilled in the art. Note that, Wu's process involves a sequence of steps including a selective oxidizing step to form oxide layer 309a (col. 9, lines 27-28), an implantation step to form source/drain region 313a (Fig. 4F(a)), and an annealing step to redistribute (also known in the art as to activate) the implanted doping impurities (col. 10, lines 1-2).

Thus, the semiconductor substrate has to be transferred from the oxidation furnace to an implantation apparatus and then back to the annealing furnace, that is the oxidation and annealing processes are carried out under an ex-situ method.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Pat. 6,599,821) in view of Wu (U.S. Pat. 6,455,383).

Lee teaches a method for fabricating a semiconductor device comprising the steps of: forming a stack layer of a gate layer (201), a poly-silicon layer (202), a tungsten layer (203), and a hard mask (204) sequentially deposited on a semiconductor substrate (200); selectively oxidizing only the poly-silicon layer (202) of the stack layer; heat treating the stack layer; and forming a gate sealing insulation layer (208) on the heat treated stack layer. See Fig. 2D and related text for the materials of layers 202 and 203. See col. 4, lines 13-25 for the selective oxidizing step and the annealing step (corresponds to the claimed heat treating step). Note that, since the selective oxidizing process and the annealing process of the reference are simultaneously performed, the stress exerted during the selective oxidizing process would inherently released by the annealing process, absent evidence to the contrary.

Lee differs from the claim in not disclosing that insulating sidewall spacer 208 is of a nitride layer.

Wu teaches gate sidewall spacers of silicon nitride are formed by LPCVD (col. 10, lines 3-4).

It would have been obvious to one of ordinary skill in the art to form the insulating sidewall spacer 208 in Lee by depositing a LPCVD silicon nitride layer as suggested by Wu because such is known in the art, and the application of a known process to make the same would have been within the level of one skilled in the art.

6. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Wu as applied to claim 1 above, and further in view of Eichman et al. (U.S. Pat. 5,308,655).

The combination of Lee and Wu teaches a process as noted above including an annealing step (corresponds to the claimed heat treatment) and a nitride deposition step by LPCVD (corresponds to the claimed forming a gate sealing nitride layer).

The combined process differs from the claims in not disclosing:

a) the annealing step and the deposition step are carried out under an in-situ method (claim 2), and b) the annealing step and the deposition step are carried out in two different LPCVD furnaces under an ex-situ method (claim 8).

Eichman et al. teach a process in which a deposition step and an annealing step can be carried out under an in-situ method (col. 2, line 63) or alternatively

the deposition step and the annealing step can be carried out in two different LPCVD furnaces under an ex-situ method (col. 3, lines 46-49).

It would have been obvious to one of ordinary skill in the art to carry out the annealing step and the deposition step under an in-situ method or an ex-situ method because it is known that in situ processing is desirable for minimizing exposure of the wafer to particulates and oxygen outside the process chamber environment, and the ex-situ method is taught to produce the same result as in the in-situ method provided that the environment outside process chambers is controlled in a non-contaminated condition.

Allowable Subject Matter

7. Claims 3-7, 9-13 and 16-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claim 3 and its dependent claims are allowable over prior art of record because prior art fails to teach or suggest, either singly or in combination, the claimed limitations regarding increasing LPCVD furnace temperature from room temperature to a target temperature and keeps the target temperature in a vacuum ambient in the heat treating step and then decreasing the LPCVD furnace

temperature from the target temperature for the heat treating to a target temperature for depositing the gate sealing nitride layer in the step of depositing the gate sealing nitride layer.

Claim 9 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding the heat treating is performed by increasing a temperature of a first LPCVD furnace from room temperature to a target temperature and keeping the target temperature in a vacuum ambient and then unloading the substrate after decreasing the temperature of the first LPCVD furnace to room temperature, and depositing the gate sealing nitride layer after moving the unloaded substrate in the first LPCVD furnace to a second LPCVD furnace.

Claim 16 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding depositing the gate sealing nitride layer in a first LPCVD furnace and heat treating the substrate in a second LPCVD furnace by increasing a temperature of the second LPCVD furnace from room temperature to a target temperature and keeping the target temperature in a vacuum or inert gas ambient and then unloading the substrate after decreasing the temperature of the second LPCVD furnace to room temperature.

Claim 17 and its dependent claims are allowable because prior art of record fails to teach or suggest the claimed limitations regarding depositing the gate sealing nitride layer in the LPCVD furnace then heat treating the substrate in an

annealing furnace by increasing a temperature of the annealing furnace from room temperature to a target temperature and keeping the target temperature in a vacuum or inert gas ambient and unloading the substrate after decreasing the temperature of the annealing furnace.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

8/16/04

